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1 Si-emulation: system verification using simulation and emulation

Zan Yang; Byeong Min; Gwan Choi;

Test Conference, 2000. Proceedings. International, 3-5 Oct. 2000

Pages: 160 - 169

[Abstract] [PDF Full-Text (700 KB)] IEEE CNF

2 Improving the quality of controls and reducing costs for on-site adjustments with emulation:an example of emulation in baggage handling

Rengelink, W.; Saanen, Y.A.;

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3 Emulation of the Sparcle microprocessor with the MIT Virtual Wires emulation system

Dahl, M.; Babb, J.; Tessier, R.; Hanono, S.; Hoki, D.; Agarwal, A.; FPGAs for Custom Computing Machines, 1994. Proceedings. IEEE Workshop on , 10-13 April 1994

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4 A Transaction-Based Unified Architecture for Simulation and Emulation

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5 A layered adaptive verification platform for simulation, test, and emulation

Zambaldi, M.; Ecker, W.; Henftling, R.; Bauer, M.;



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1 Predicting error rate for microprocessor-based digital architectures through C.E.U. (Code Emulating Upsets) injection

Velazco, R.; Rezgui, S.; Ecoffet, R.;

Nuclear Science, IEEE Transactions on , Volume: 47 , Issue: 6 , Dec. 2000

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2 Using background modes for testing, debugging and emulation of microcontrollers

Melear, C.;

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3 Emulation techniques for microcontrollers with internal caches and multiple execution units

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LeVine, M.J.; Stancu, S.; Haeberli, C.; Tremblet, L.; Beuran, R.; Meirosu, C.; Dobinson, R.W.; Martin, B.; Knezo, E.; Beck, H.P.; Hauser, R.; Botterill, D.; Nuclear Science, IEEE Transactions on , Volume: 51 , Issue: 3 , June 2004 Pages: 539 - 544

[Abstract] [PDF Full-Text (472 KB)] IEEE JNL

2 Configurable multilayer CNN-UM emulator on FPGA

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[Abstract] [PDF Full-Text (552 KB)] IEEE JNL

3 Design of FPGA-based emulator for series multicell converters using cosimulation tools

Ruelland, R.; Gateau, G.; Meynard, T.A.; Hapiot, J.-C.;

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